WHAT IS CLAIMED IS:

1. A method of dividing a configuration space, applied to a computer system comprising a microprocessor, a north bridge control chip, a first bus, a south bridge control chip, and a second bus, wherein the first bus is coupled to the north bridge control chip and south bridge control chip and the south bridge chip is further coupled to the second bus, the method comprising:

providing a first actual configuration space in the north bridge control chip to store a plurality of configuration values relating to the a plurality of devices connected to the north bridge control chip;

providing a second actual configuration storage space in the south bridge control chip to store a plurality of configuration values relating to the second bus; and

transmitting a write operation cycle to both the north bridge control chip and the south bridge control chip when the microprocessor is performing the write operation cycle related to the configuration spaces, wherein:

the first actual configuration space is written to only when the write operation cycle is addressed to the first actual configuration space; and

the second actual configuration space is written to only when the write operation cycle is addressed to the second configuration storage space;

when the microprocessor is performing a read operation cycle related to the configuration spaces,

selecting data read from the first actual configuration space only when the read operation cycle is addressed at the first actual configuration space; and

selecting data read from the second actual configuration space only when the read operation cycle is addressed at the second actual configuration storage space.

2. The method according to claim 1, further comprising:

providing a selector in the north bridge control chip, to select data read from either the first or the second actual configuration space when the microprocessor is performing the read operation cycle related to the configuration space.

3. The method according to claim 1, wherein the configuration values of the configuration space in the north bridge control chip comprises a plurality of settings of the microprocessor and a memory system.

4. The method according to claim 1, wherein the first bus comprises a high speed private bus.

5. The method according to claim 1, wherein the second bus comprises a PCI bus.

6. A method of dividing a configuration space, applied to a computer system comprising a microprocessor, a host bus, a north bridge control chip, a high speed private bus, a PCI bus, a south bridge control chip, a memory bus, and a memory system, wherein the host bus is coupled to the microprocessor and the north bridge control chip, the memory bus is coupled to the north bridge control chip and the memory system, the high speed private bus is coupled to the north and the south bridge control chips, and the south bridge control chip is coupled to the PCI bus, the method comprising:

providing a configuration storage space located in the north bridge control chip, wherein the configuration space includes a first actual configuration space to store a plurality of configuration values relating to the microprocessor and the memory system and a first duplicated copy of configuration space;

providing a configuration space located in the south bridge control chip, wherein the configuration space includes a second actual configuration storage space actual to store a plurality of configuration values relating to the PCI bus and a second duplicated

copy of configuration space;

providing a selector, comprising a first input terminal and a second input terminal, wherein the first input terminal and the second terminal are coupled respectively to the configuration spaces in the north bridge control chip and the south bridge control chip, the selector further comprising an output terminal coupled to the main bus;

transmitting a write request to the second duplicated copy of configuration space when the microprocessor is performing the write operation on the first actual configuration space;

transmitting a write request to the first duplicated copy of configuration space when the microprocessor is performing the write operation on the second actual configuration space;

outputting the first input terminal of the selector to the output terminal thereof when the processor is performing a read operation on data stored in the first actual configuration space; and

outputting the second input terminal of the selector to the output terminal thereof when the processor is performing a read operation on data stored in the second actual configuration space.

7. A system of dividing a configuration space, comprising:

a microprocessor;

a north bridge control chip, coupled to the microprocessor;

a first bus, coupled to the north bridge control chip;

a south bridge control chip, coupled to the first bus; and

a second bus, coupled to the south bridge control chip; wherein:

the north bridge control chip comprises a first actual configuration space to store a

plurality of configuration values relating to a plurality of device connected to the north bridge control chip, and the south bridge control chip comprises a second actual configuration space to store a plurality of configuration values relating to the second bus;

a write operation cycle is output to both the north and south bridge control chips when the microprocessor is performing a write operation cycle related to the configuration storage spaces;

only the first actual configuration space is written when the write operation cycle is addressed to the first actual configuration space; and

only the second actual configuration space is written when the write operation cycle is addressed to the second actual configuration space;

when the microprocessor is performing a read operation cycle related to the configuration space:

data read from the first actual configuration space is selected when the read operation cycle is addressed to the first actual configuration space; and

data read from the second actual configuration space is selected when the read operation cycle is addressed to the second actual configuration space.

8. The system according to claim 7, wherein the north bridge control chip comprises a selector to select the data read from either the first actual configuration space or the second actual configuration space when the microprocessor is performing the read operation cycle.

9. The system according to claim 7, wherein the configuration values of the first actual configuration space in the north bridge control chip comprises a plurality of settings of the microprocessor and a memory system.

10. The system according to claim 7, wherein the first bus comprises a high speed

private bus.

11. The system according to claim 7, wherein the second bus comprises a PCI bus.

12. The system according to claim 7, wherein the north bridge control chip further comprises a first duplicated copy of configuration storage space mapping to the second actual configuration space.

13. The system according to claim 7, wherein the south bridge control chip further comprises a second duplicated copy of configuration space mapping to the first actual configuration space.